What is claimed is:

1. A method for determining a phase angle relationship between capacitive test points, comprising the steps of:

receiving a first waveform indicating the presence of a voltage at first capacitive test point;

receiving a second waveform indicating the presence of a voltage at a second capacitive test point;

comparing the first and second waveforms with respect to time;

measuring a phase angle difference between the first and the second waveforms; and

determining the phase angle relationship between the first and the second capcitive test points based on said phase angle difference.

2. The method of claim 1, further comprising :

displaying the phase angle relationship between the first and second capacitive test points.

3. The method of claim 1, wherein the phase angle difference determines whether the voltages at the first and the second capacitive test points are in phase.

4. The method of claim 1, wherein the phage angle difference determines whether the voltages at the first and the second capacitive test points are out of phase.

5. The method of claim 1, wherein the phase angle difference is independent of voltage values at the first and second capacitive test points.

6. The method of claim 1, wherein the phase angle difference is independent of contamination at first and second capacitive test points.

7. A capacitive test point voltage and phasing detector comprising:

a first detector member having a longitudinal extending first probe with a pointed upper end and a lower end, wherein the upper end is configured to engage with a first capacitive test point, a module positioned between the upper and the lower end of the first probe, wherein the module is configured to sense the voltage at each capacitive test point and the phase angle difference between two capacitive test points, a first universal adapter connected to the lower end of the first probe and a first non-conductive stick attached to the first universal adapter;

a second detector member having a longitudinal extended second probe with an upper end and a lower end, wherein the upper end is configured to engage with a second capacitve test point, a probe jack mounted on said second probe, a second universal adapter connected to the lower end of the second probe and a second non-conductive stick attached to the second universal adapter; and

a lead wire having two ends connected between the first and the second detector member to provide an electrical communication between the first and the second detector member.

8. The capacitive test point voltage and phasing detector of claim 7, wherein the probe jack is electrically engaged to one of the ends of the lead wire.

9. The capacitive test point voltage and phasing detector of claim 7, wherein said module further comprises:

a ground jack for connecting a ground lead to the system ground;

a phase 2 jack electrically engaged to the other end of the lead wire;

a power display including a switch for controlling power of the capacitive test point voltage and phasing detector;

a phase 1 display indicating the presence of voltage at the first capactiive test point;

a phase 2 display indicating the presence of voltage at the second capacitive test point; and

a phasing display indicating the phase relationship between the voltages at the

first and second capactive test points.

10. The capacitive test point voltage and phasing detector of claim 9, wherein the phasing display comprises an in display indicating the voltages at the two capacitive test points are in phase with each other and an out display indicating the voltages at the two capacitive test points are out of phase with each other.

11. The capacitve test point voltage and phasing detector of claim 9, wherein the power display is a light emitting diode.

12. The capacitive test point voltage and phasing detector of claim 9, wherein the phase 1 display is a light emitting diode.

13. The capacitve test point voltage and phasing detector of claim 9, wherein the phasing display is a light emitting diode.

14. The capacitve test point voltage and phasing detector of claim 10, wherein the in display is a light emitting diode.

15. The capacitive test point voltage and phasing detector of claim 10, wherein the out display is a light emitting diode.

16. The capacitive test point voltage and phasing detector of claim 9, wherein the switch comprises of first, second and third positions.

17. The capacitive test point voltage and phasing detector of claim 16, wherein the first position indicates that the detector is turned off.

18. The capacitive test point voltage and phasing detector of claim 16, wherein the second position indicates that the detector is turned on.

19. The capacitive test point voltage and phasing detector of claim 16, wherein the third position indicates that the detector is turned on and is in a sensitive mode.

20. The capacitive test point voltage and phasing detector of claim 19, wherein the sensitive mode provides an accurate indication of the presence of voltage at the two capacitive test points independent of contamination at the first and second capacitive test points.

21. The capacitive test point voltage and phasing detector of claim 19, wherein the sensitive mode provides an accurate indication of the presence of voltage at the two capacitive test points independent of voltage values at the first and second capacitive test points.

22. An apparatus for detecting a phase angle relationship between two capacitive test points, comprising:

a first amplifier having an input and output, including a first resistor connected to the input of the first amplifier for providing a low input impedance at the first amplifier;

a first voltage channel connected to the input of the first amplifier for receiving first voltage signal from a first capacitive test point;

a second amplifier having an input and output, including a second resistor connected to the input of the second amplifier for providing a low input impedance at the second amplifier;

a second voltage channel connected to the input of the second amplifier for receiving second voltage signal from a second capacitive test point;

a power on self-tester coupled to send test voltage signals to the first and second amplifiers for testing the functionality of the apparatus;

a first output voltage signal received from the output of the first amplifier;

a second output voltage signal received from the output of the second amplifier;

a phase detector coupled to receive the first and second output voltage signals, wherein the phase detector determines a phase angle difference between the first and the second output voltage signals;

a state detector coupled to receive the first and second output voltage signals; and

a switch connected to the state detector.

23. The apparatus of claim 22, wherein the phase angle difference determines whether voltages at the first and second capacitive test points are in phase.

24. The apparatus of claim 22, wherein the phase angle difference determines whether voltages at the first and second capacitive test points are out of phase.

25. The apparatus of claim 22, wherein the phase angle difference is independent of voltage values at the first and the second capacitive test points.

26. The apparatus of claim 22, wherein the phase angel difference is independent of the contamination at the first and the second capacitive test points.

27. The apparatus of claim 22, wherein the first and second resistors are in the magnitude of tens of kiloohms.

28. The apparatus of claim 27, wherein the first and second resistors are measured at 22 kiloohms.

29. The apparatus of claim 22, wherein the state detector accurately indicates that a voltage is present at the first and second capacitive test points.

30. The apparatus of claim 29, wherein the state detector sends a signal to the phase detector when the voltage is present at the first and second capacitive test points.